

CCD area image sensor

S8665-0909

Four-stage thermoelectric cooled, back-thinned FFT-CCD



S8665-0909 is an FFT-CCD area image sensor featuring low noise and low dark current (MPP mode operation). The output charge can be integrated for long periods of time even at low light levels, allowing a wide dynamic range.

S8665-0909 uses a four-stage thermoelectric cooler that cools the CCD down to $-50\text{ }^{\circ}\text{C}$ when operated at room temperatures, achieving even lower noise and dark current.

Features

- Four-stage TE-cooled
- Number of active pixels: 512 (H) \times 512 (V)
- Pixel size: $24 \times 24\text{ }\mu\text{m}$
- 100 % fill factor
- Wide dynamic range
- Low dark current
- Low readout noise
- MPP operation

Applications

- Astronomy
- Scientific measuring instrument
- UV imaging
- For low-light-level detection requiring

■ Selection guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm(H) \times mm(V)]
S8665-0909	Four-stage TE-cooled	532 \times 520	512 \times 512	12.288 \times 12.288

■ Specifications

Parameter	Specification
CCD structure	Full frame transfer
Fill factor	100 %
Cooling	Four-stage TE-cooled
Number of pixels	532 (H) \times 520 (V)
Number of active pixels	512 (H) \times 512 (V)
Pixel size	24 (H) \times 24 (V) μm
Active area	12.288 (H) \times 12.288 (V) mm
Vertical clock phase	2 phase
Horizontal clock phase	2 phase
Output circuit	One-stage MOSFET source follower
Package	28 pin metal package
Window	AR coated sapphire

■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	VOD	-0.5	-	+25	V
RD voltage	VRD	-0.5	-	+18	V
ISV voltage	Visv	-0.5	-	+18	V
ISH voltage	VISH	-0.5	-	+18	V
IGV voltage	VIG1V, VIG2V	-10	-	+15	V
IGH voltage	VIG1H, VIG2H	-10	-	+15	V
SG voltage	VSG	-10	-	+15	V
OG voltage	VOG	-10	-	+15	V
RG voltage	VRG	-10	-	+15	V
TG voltage	VTG	-10	-	+15	V
Vertical clock voltage	VP1V, VP2V	-10	-	+15	V
Horizontal clock voltage	VP1H, VP2H	-10	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Output transistor drain voltage	VOD	18	20	22	V	
Reset drain voltage	VRD	11.5	12	12.5	V	
Output gate voltage	VOG	1	3	5	V	
Substrate voltage	VSS	-	0	-	V	
Test point (vertical input source)	Visv	-	VRD	-	V	
Test point (horizontal input source)	VISH	-	VRD	-	V	
Test point (vertical input gate)	VIG1V, VIG2V	-8	0	-	V	
Test point (horizontal input gate)	VIG1H, VIG2H	-8	0	-	V	
Vertical shift register clock voltage	High	VP1VH, VP2VH	4	6	8	V
	Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	4	6	8	V
	Low	VP1HL, VP2HL	-9	-8	-7	
Summing gate voltage	High	VSGH	4	6	8	V
	Low	VSGL	-9	-8	-7	
Reset gate voltage	High	VRGH	4	6	8	V
	Low	VRGL	-9	-8	-7	
Transfer gate voltage	High	VTGH	4	6	8	V
	Low	VTGL	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	1	MHz
Vertical shift register capacitance	CP1V, CP2V	-	6,400	-	pF
Horizontal shift register capacitance	CP1H, CP2H	-	120	-	pF
Summing gate capacitance	CSG	-	7	-	pF
Reset gate capacitance	CRG	-	7	-	pF
Transfer gate capacitance	CTG	-	150	-	pF
Charge transfer efficiency *1	CTE	0.99995	0.99999	-	-
DC output level *2	Vout	12	15	18	V
Output impedance *2	Zo	-	3	-	kΩ
Power consumption *2 *3	P	-	15	-	mW

*1: Charge transfer efficiency per pixel, measured at half of the full well capacity.

*2: The values depend on the load resistance. (Typical, VOD=20 V, Load resistance=22 kΩ)

*3: Power consumption of the on-chip amplifier.

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit			
Saturation output voltage	Vsat	-	-	Fw × Sv	-	V			
Full well capacity	Vertical	Fw	*4	150	300	-	ke ⁻		
	Horizontal			300	600	-			
CCD node sensitivity	Sv	*5	1.8	2.2	-	μV/e ⁻			
Dark current (MPP mode)	+25 °C	DS	*6	-	4,000	12,000	e ⁻ /pixel/s		
	0 °C			-	200	600			
	-30 °C			-	3	9			
Readout noise	Nr	*7	-	8	12	e ⁻ rms			
Dynamic range	Line binning	DR	*8	-	75,000	-	-		
	Area scanning			-	37,500	-			
Spectral response range	λ	-	-	200 to 1100	-	nm			
Photo response non-uniformity	PRNU	*9	-	-	±10	%			
Blemish	Point defect	-	-	-	10	-			
	Cluster defect						*11	-	3
	Column defect						*12	-	0

*4: Large horizontal full well capacity for line binning operation.

*5: V_{OD}=20 V, load resistance=22 kΩ.

*6: Dark current nearly doubles for every 5 to 7 °C increase in temperature.

*7: -40 °C, operating frequency is 80 kHz.

*8: Dynamic range DR=Full well capacity/Readout noise

*9: Measured at half of the full well capacity output.

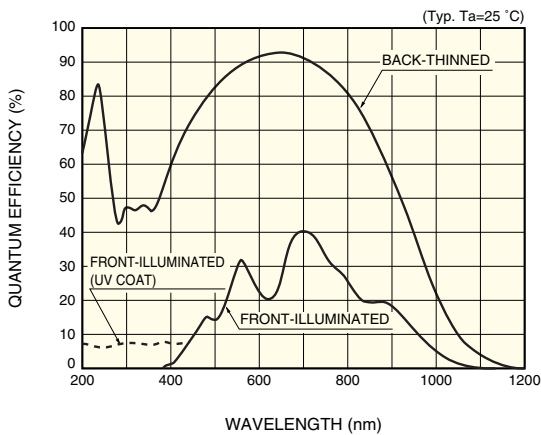
$$\text{Photo response non-uniformity (PRNU) [\%]} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

*10: White spots > 3 % of full well at 0 °C after Ts=1 s, Black spots > 50 % reduction in response relative to adjacent pixels.

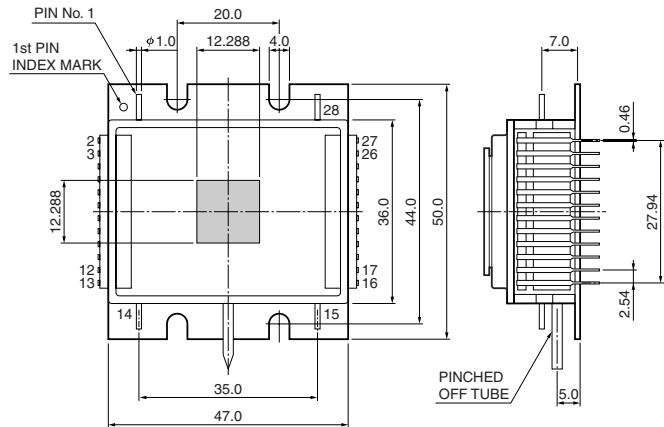
*11: Continuous 2 to 9 point defects.

*12: Continuous ≥ 10 point defects.

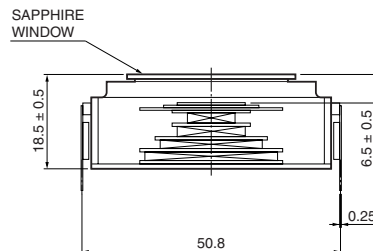
■ Spectral response (without window) *13



■ Dimensional outline (unit: mm)

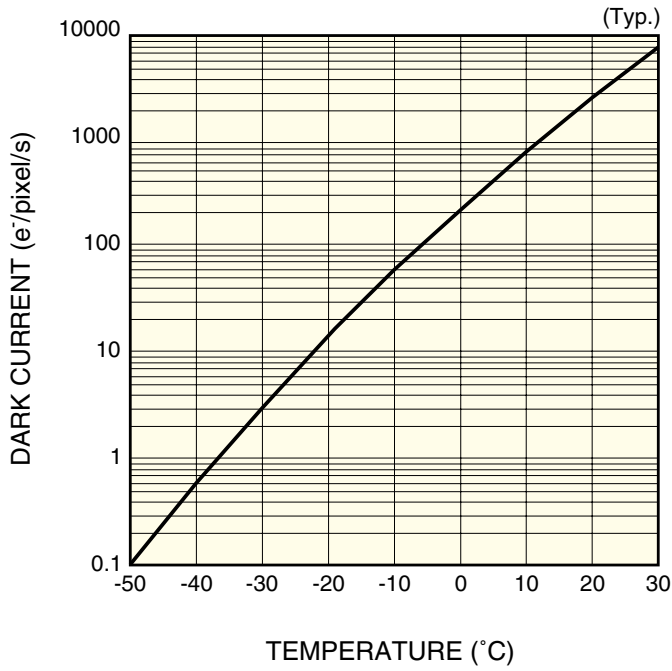


*13: Spectral response with sapphire window is decreased by the transmittance



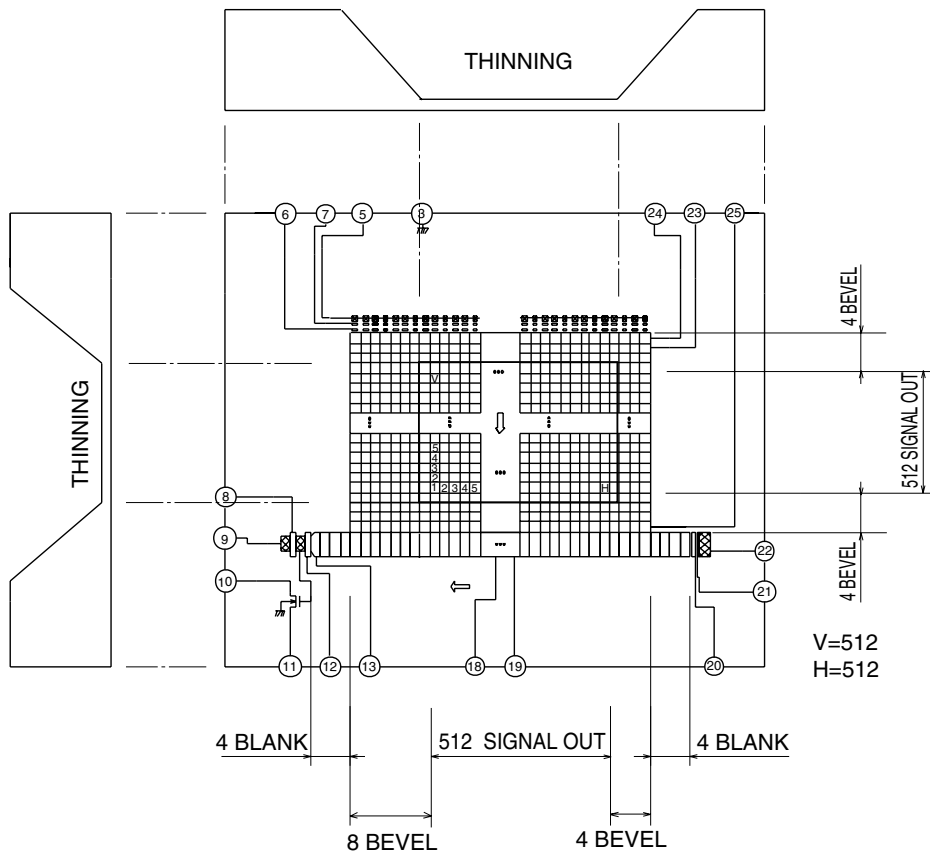
KMPDA0142EB

■ Dark current vs. temperature



KMPDB0037EB

■ Device structure



KMPDC0075EB

■ PIN connections

Pin No.	Symbol	Description	Remark
1	P-	TE-cooler-	
2	NC		
3	SS	Substrate (GND)	
4	NC		
5	ISV	Test point (vertical input source)	Shorted to RD
6	IG2V	Test point (vertical input gate-2)	Shorted to 0 V
7	IG1V	Test point (vertical input gate-1)	Shorted to 0 V
8	RG	Reset gate	
9	RD	Reset drain	
10	OS	Output transistor source	
11	OD	Output transistor drain	
12	OG	Output gate	
13	SG	Summing gate	Same timing as P2H
14	P+	TE-cooler+	
15	TSH1	Temperature sensor (hot side)	
16	TSC1	Temperature sensor (cool side)	
17	TSC2	Temperature sensor (cool side)	
18	P2H	CCD horizontal register clock-2	
19	P1H	CCD horizontal register clock-1	
20	IG2H	Test point (horizontal input gate-2)	Shorted to 0 V
21	IG1H	Test point (horizontal input gate-1)	Shorted to 0 V
22	ISH	Test point (horizontal input source)	Shorted to RD
23	P2V	CCD vertical register clock-2	
24	P1V	CCD vertical register clock-1	
25	TG	Transfer gate	Same timing as P2V *14
26	NC		
27	NC		
28	TSH2	Temperature sensor (hot side)	

*14: TG is an isolation gate between vertical register and horizontal resistor.
 In standard operation, the same pulse of P2V should be applied to the TG.

■ Specifications of built-in TE-cooler

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal resistance	Rint	Ta=27 °C	-	1.6	-	Ω
Maximum current *17	I _{max}	Th *18=27 °C ΔT *19=ΔT _{max}	-	-	4.4	A
Maximum voltage	V _{max}	Th*18=27 °C ΔT=ΔT _{max} I=I _{max}	-	-	7.4	V
Maximum heat absorption *20	Q _{max}	T _c *21=Th *19=27 °C I=I _{max}	-	-	3.0	W
Maximum temperature at hot side	-		-	-	50	°C
CCD temperature	-	Ta=25 °C	-	-50	-30	°C

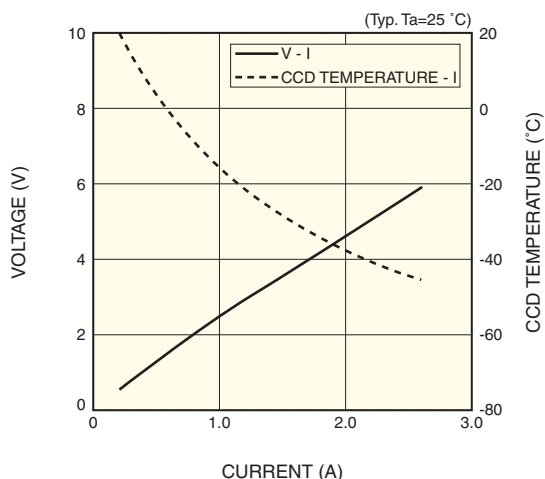
*17: If the current is greater than I_{max}, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not a damage threshold. To protect the thermoelectric cooler (Peltier element) and maintain stable operation, the supply current should be less than 60 % of this maximum current.

*18: Temperature at hot side of thermoelectric cooler.

*19: ΔT=Th - T_c

*20: This is a theoretical heat absorption level that offsets the temperature difference in the Peltier element when the maximum current is supplied to the unit.

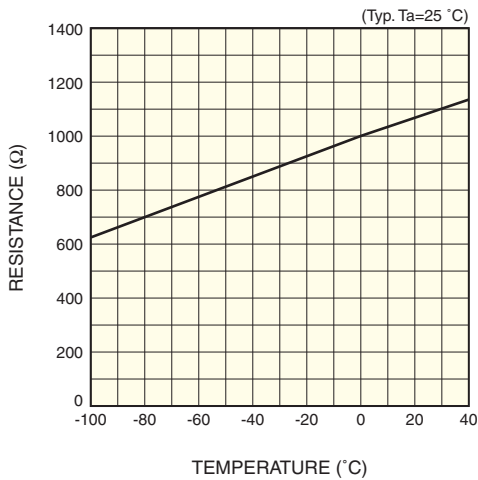
*21: Temperature at cool side of thermoelectric cooler.



KMPD80222EA

■ Specifications of built-in temperature sensors

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resistance at cool side	R _c	T=0 °C	-	1,000	-	Ω
Temperature coefficient of resistance at cool side	-	-	-	0.00375	-	Ω/Ω
Resistance at hot side	R _h	T=0 °C	-	1,000	-	Ω
Temperature coefficient of resistance at hot side	-	-	-	0.00385	-	Ω/Ω



KMPDB0108EA

■ **Precaution for use (electrostatic countermeasures)**

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ **Element cooling/heating temperature incline rate**

Element cooling/heating temperature incline rate should be set at less than 5 K/min.